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(54) Structure and fabrication method for schottky and ohmic electrodes onto semiconductor devices

(57) A novel electrode structure for Schottky electrodes and Ohmic electrodes and novel methods of fabricating electrodes by freely controlling electric characteristics of electrodes on semiconductors. Interface states density of a semiconductor (11) after deposition of an electrode metal (13, 14) is decreased by flattening the surface of the semiconductor on an atomic level to freely control the Schottky barrier height. The method can realize an ideal Ohmic electrode having a Schottky barrier height of substantially zero. The Schottky barrier height is varied freely by decreasing the interface level density and selecting work function of the electrode metal. The method can provide stable Schottky and Ohmic electrodes (13, 14) without need of heat treatment. Further, the method can provide Ohmic electrodes without high concentration doping.

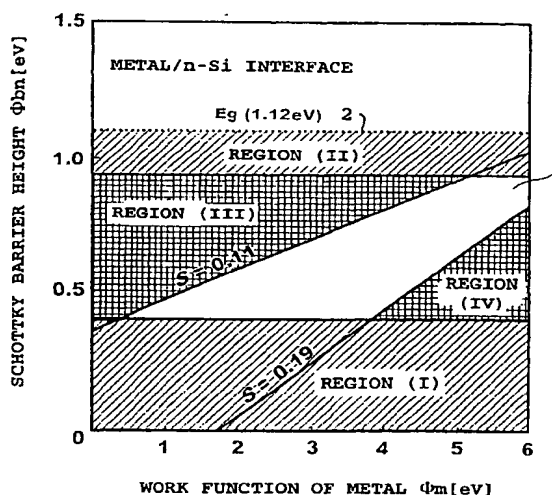


FIG. 2

Description

The present invention relates to an electrode provided on a semiconductor and a method for fabricating an electrode on a semiconductor. The present invention is applicable to various fields of industry which involve fabrication of electrodes on semiconductors. For example, the present invention can be applied to various semiconductor devices such as microprocessors, memories, power devices and the like.

In conventional fabrication methods of electrodes on semiconductors, rectifying potential barriers, i.e., Schottky barriers, which will appear on the interfaces between electrode metals and semiconductors, have been impossible to control their magnitude. Hence, it has been impossible to artificially control the rectifying properties and conductivities of all the electrodes including not only those semiconductor devices whose performance depends directly on the heights of Schottky barriers, such as Schottky diodes as typical examples, but also those electrodes in the semiconductor devices thus far fabricated. The Schottky barrier height and leakage current, which is an indicator of important performance of interface on the device, inconveniently vary to a greater extent depending on combination of metals and semiconductors as well as on the process in which the interface is formed. Conventionally, this problem has been solved empirically. That is, when a new semiconductor has been developed, a method for fabricating an electrode on the semiconductor has been investigated and developed for each metal one after another until a suitable one is obtained. In other words, going into detail, there have conventionally been developed unique fabrication methods for fabricating electrodes adapted for respective combinations of semiconductors and electrode metal materials. Because of having had to resort to empirical rule, methods for fabricating electrodes differ from institution to institution or from manufacturer to manufacturer. There has been established no fabrication method for fabricating electrodes which method can be uniformly applied to any or most of electrode metal/semiconductor combinations. Under the circumstances, development of electrodes has needed much human and monetary resources for investigation. In all the semiconductor device fabrication technology inclusive of technologies for fabricating integrated semiconductor devices such as VLSIs and the like, only the technology for forming electrodes has remained as a unit technology that is out of reach of successful efforts for free designing.

More specific explanation will be made as to how to fabricate electrodes for Schottky electrodes and Ohmic electrodes, respectively.

First, in the case of Schottky electrodes, it was almost impossible to control their Schottky barrier height and, hence there was no other way than accept such non-controlled values as they are. For example, silicon Schottky diodes have almost fixed barrier heights on the order of about 0.5 to about 0.7 eV. While use of different metals or application of heat to cause interface reaction will vary barrier height to some extent, the width of change in barrier height is at most about 0.2 eV. Thus, in Schottky devices, the Schottky barrier height, which is the most important indicator for the device characteristics, cannot be controlled freely.

In the case of Ohmic electrodes, a severer problem arises. That is, electrode fabrication inevitably results in the formation of a Schottky barrier whose interface usually shows rectifying resistance. As a result, formation of a conductive Ohmic electrode, which is contrary to the fabrication of an electrode having a rectifying resistance, requires in principle a very difficult technique. Practically, in fabrication of almost all of the Ohmic electrodes fabricators have presupposed presence of a Schottky barrier in the interface between the electrode metal and semiconductor and then taken a measure to allow a leakage current to flow in the barrier.

There have been known several methods for increasing a leakage current. For example, a method for fabricating a device in which impurity ions are doped to extremely increase the concentration of electrons or holes which contribute to conductivity in the vicinity of the surface of the semiconductor (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M. Murakami: Materials Science Reports, 5, 273 (1990), P.A. Barnes and A.Y. Cho, Appl. Phys. Lett., 33, 651 (1978), and T. Uemoto: Jpn. J. Appl. Phys., 34, L7 (1995)). This reduces the width of the Schottky barrier, i.e., decreases the thickness of the depletion layer and, hence, a leakage current in the form of tunneling current, can be flown in the thin depletion layer. However, in the case of SiC, GaN and the like new semiconductor materials that are under development are usually difficult to dope with impurities at high concentrations so that electrodes having sufficiently low resistance cannot be obtained in most cases. The above-described method is not simple nor convenient in some cases since it requires an ion implanting apparatus or an electric oven for diffusing impurities in gaseous phases. Furthermore, the concentration of impurities has an upper limit at about 10^{20}cm^{-3} . This automatically determines the minimum width of the depletion layer and, hence, sets technical limits to the interface resistance of an Ohmic electrode to be realized. Theoretically, this approach is unsuccessful in making the interface resistance of the Ohmic electrode to be zero. In addition, there may occur reflection of electrons or holes between the high concentration doped region and the low concentration doped substrate. This reflection of carriers increases the resistance of the electrode. From these, the interface resistance of an Ohmic electrode fabricated on a silicon substrate is limited to about $10^{-8}\ \Omega\text{cm}^2$ based on the technical restrictions as described above.

Another method for fabricating an Ohmic electrode is to heat the electrode to decrease its resistance (cf., e.g., E. H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M.

Murakami: Materials Science Reports, 5, 273 (1990), H.C. Card: IEEE Trans. Electron Devices, ED-23, 538 (1976), T.C. Shen, G.B. Gao, and H. Morkoç: J. Vac. Sci. Technol., B10, 2113 (1992), N. Braslau, J.B. Gunn, and J.L. Staples: Solid-State Electronics, 10, 381 (1967), J. Appl. Phys., 77, 1317 (1967), and J. Crofton, P.G. McMullin, J.R. Williams, and M.J. Bozack: J. Appl. Phys., 77, 1317 (1995)). In this method, after the electrode metal is deposited, heat treatment is carried out so that there occurs interface chemical reaction between the metal and the semiconductor and metallization of the semiconductor proceeds in the vicinity of the interface. This induces impurity level or defect level in the depletion layer of the Schottky barrier. These levels generate leakage current. This method is simple and can be used in combination with high concentration doping. Because of the advantages, the method is used without fail in the conventional process of fabricating electrodes. However, interface reaction is complicated since it differs from a metal/semiconductor system to another and the mode of reaction varies widely depending on temperature and time of heat treatment. In some reaction systems, it is often the case that heating results in the formation of good Schottky barrier, which means heating does not always enhance Ohmicity (cf., e.g., S. Zaima, T. Yamauchi, Y. Koide, and Y. Yasuda: Appl. Surf. Sci., 70, 624 (1993)). This is a decisive defect of the above-described heating method.

Still another approach is to grow on a first semiconductor a crystal of a second semiconductor having a bandgap smaller than that of the first semiconductor so that the highest possible Schottky barrier height can be decreased to facilitate the formation of Ohmic contact (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M. Murakami: Materials Science Reports, 5, 273 (1990), and T.C. Shen, G.B. Gao, and H. Morkoç: J. Vac. Sci. Technol., B10, 2113 (1992)). This method involves heteroepitaxy of a semiconductor and, hence, its application is limited to semiconductor systems which allow heteroepitaxy.

Further, heteroepitaxy itself is a high technology which requires a complicated manufacturing process, which increases production costs. Therefore, the method is suited to a very limited range of semiconductor materials, more particularly, new semiconductor materials having wide bandgaps, such as GaN and the like, which are difficult to dope with high concentration doping of impurities.

The above-described three methods use large process apparatus suitable for fabricating devices and thus are not simple. Accordingly, in early stages of research and development for evaluating electric properties of materials or developing various devices, simpler means such as scratching of semiconductor or the like is used (here, by the term "scratching" is meant to hurt the surface of a semiconductor with a diamond needle or the like to coarsen it (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988)). On a coarse surface, a lot of structural defects are induced which increase leakage current. This method is quite inconvenient for making fine structures in the fabrication of semiconductor devices. In most cases, no good interface resistance can be obtained.

As described above, electrodes have been fabricated based on empirical rules. The primary reason for this is a lack of common or uniform understanding of the mechanism in forming a metal/semiconductor interface potential barrier. Uncontrollability of Schottky barriers and complexity of the mechanism of Ohmic contact formation which is attributable thereto would be due to the fact that Schottky barrier height is by nature fixed to a certain level. Fixation of Schottky barrier height of a semiconductor is equivalent to the fact that the Fermi level is fixed in the bandgap of the semiconductor on the metal/semiconductor interface. The fixation of Fermi level is usually referred to pinning of the Fermi level. The pinning of the Fermi level occurs as a result of generation of electron level in the bandgap of a semiconductor on the interface between the metal and the semiconductor. Carriers flow from bulk to the interface, i.e., electrons in the case of n-type semiconductor or holes in the case of p-type semiconductor flow from the bulk semiconductor to the interface and the carriers are trapped therein to create an electric double layer of the semiconductor bulk and the interface, i.e., a potential barrier or Schottky barrier.

Reviewing the development of Schottky barrier, in 1947, J. Bardeen stated that the interface level is caused by electronic level due to dangling bonds and the like existing on the surface of the semiconductor (cf. J. Bardeen: Phys. Rev., 71, 717 (1947)). Thereafter, however, in view of the impossibility of controlling the surface level density accurately by the technology available at that time, the leading view was that surface level density was uncontrollable and intrinsic to the material concerned, and interface electron level embedded in a solid should be an essential electron level that was more difficult to control than the surface level. The belief that pinning was intrinsic to materials and cannot be controlled artificially has led to a theory of MIGS (Metal-induced Gap States) which explains a cause of generation of interface levels (cf. V. Heine: Phys. Rev., 138, A1689 (1965)). According to this theory, interface levels are induced when a metal approaches toward the semiconductor. Since 1965 when V. Heine proposed it, the MIGS theory has been leading to date. The MIGS theory has inhibited research of a technology which controls the height of Schottky barrier. In fact, regardless of theories, there have been unavailable high technologies that can control interface level density in actual semiconductor devices.

Concerning numerical consideration of pinning, the work which referred to Schottky barrier for the first time was by W. Schottky (cf. W. Schottky: Naturwissenschaften, 26, 843 (1938) and N.F. Mott: Proc. Camb. Philos. Soc., 34, 568 (1938)). According to Schottky, the Schottky barrier height, ϕ_{bn} , of a n-type semiconductor is given by the following equation (1):

$$\phi_{bn} = \phi_m - \chi S + C \quad (1)$$

wherein ϕ_m is a work function of the metal, χS is electron affinity of the semiconductor, C is a constant no greater than several meV. On the other hand, the Schottky barrier height of a p-type semiconductor in a pinning-free state is given by the following equation (2):

$$\phi_{bp} = E_g - (\phi_m - \chi S + C) \quad (2)$$

wherein E_g is a bandgap.

The equations (1) and (2) are called Schottky models. However, no interface has been realized that meets these equations. The actual interface is expressed by the following equation (3):

$$\phi_{bn} = S (\phi_m - \chi S) + C \quad (3)$$

wherein S is a coefficient which indicates a dependence of ϕ_{bn} on ϕ_m and $0 \leq S \leq 1$.

When $S=0$, ϕ_{bn} is constant and the interface is pinned strongly. This state is called a Bardeen barrier. On the contrary, when $S=1$, the equation (3) is the same as the equation (1) and represents a pinning-free interface according to the Schottky-Mott model. Actual interfaces fall between the both states. Heretofore, the S factor has been believed to be a physical property specific to the material concerned and, hence, beyond control.

Table 1 below summarizes values of S factor and maximum and minimum values of Schottky barrier height of representative semiconductors.

Table 1

PINNING RATIOS S OF VARIOUS KNOWN SEMICONDUCTORS AND RANGE OF SCHOTTKY BARRIER HEIGHT

SEMI- CONDUCTOR	S FACTOR	INTERCEPT PARAMETER	MINIMUM SCHOTTKY BARRIER HEIGHT [eV]	MAXIMUM SCHOTTKY BARRIER HEIGHT [eV]
Ge	$0.18 \geq S \geq 0.05^1$	$-0.23 \leq C_2 \leq 0.11^1$		
Si(001)	$0.19 \geq S \geq 0.11^1$	$-0.34 \leq C_2 \leq 0.35^1$	$0.37(\text{GdSi}_2/\text{HoSi}_2)^2$	$0.94(\text{IrSi}_3)^3$
GaAs(001)	$0.22 \geq S \geq 0.06^1$	$-0.40 \leq C_2 \leq 0.075^1$	$0.62(\text{Mg})^4$	$0.96(\text{Cu})^4$
GaP	$0.21 \geq S \geq 0.07^1$	$0.45 \leq C_2 \leq 0.80^1$		
InP	$0.37 \geq S \geq 0.24^1$	$-1.00 \leq C_2 \leq 0.81^1$		
ZnS	$0.66 \geq S \geq 0.21^1$	$-1.63 \leq C_2 \leq 0.91^1$		
ZnSe	$0.24 \geq S \geq 0.17^1$	$-0.25 \leq C_2 \leq 0.57^1$		
6H-SiC(0001)	$0.25 \geq S \geq 0.23^{5-10}$	$-3.5 \leq C_2 \leq 0.15^{5-10}$	$0.73(\text{Ti})^6$	$1.37(\text{Au})^5$

1. B.L. Sharma and S.C. Gupta, Solid State Technology, 23(6), 90 (1980).
2. K.N. Tu, R.D. Thompson, and B.Y. Tsaur, Appl. Phys. Lett. 38, 626(1981).
3. C.S. Petersson, et al., J. Appl. Phys., 50, 3357 (1979).
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6. J.R. Waldrop, et al., Appl. Phys. Lett., 62, 2685 (1993).
7. L.M. Porter, et al., Mat. Res. Soc. Symp. Proc., 287, 471 (1993).
8. L.M. Porter, et al., J. Mat. Res., 10, 26 (1995).
9. L.M. Porter, et al., J. Mat. Res., 10, 668 (1995).
10. L.M. Porter, et al., M. Mat. Res. 10, 2336 (1995).

Fig. 1 is a graphical presentation of the data in Table 1, plotting Schottky barrier height (ϕ_{bn} [eV]) against work function of a metal (ϕ_m [eV]) taking as an example of an n-type Si(001) semiconductor substrate. Fig. 1 shows that the Schottky barrier height was limited within a certain range for various metals. In Fig. 1, reference numeral 1 denotes an area representing the range in which the Schottky barrier heights of conventionally fabricated metal/n-Si interfaces fall and 2 denotes a line which represents an absolute upper limit of the Schottky barrier height of metal/n-Si interfaces corresponding to the bandgap $E_g = 1.12$ eV. With different metals, there are always upper and lower limits of the Schottky

barrier heights.

Consequently, it has heretofore been impossible to freely control the Schottky height of metal/semiconductor interfaces.

The present invention is directed to overcoming the problem of uncontrollability of the Schottky barrier height between an electrode metal and a semiconductor, which problem has been an important subject since a transistor was invented.

Also, the present invention is aimed at solving the scientific and technological problem of uncontrollability of Ohmic electrodes, which has heretofore been considered a different problem from the uncontrollability of Schottky barrier height.

Further, the present invention is intended to provide a systematic technology which can control both Schottky electrodes and Ohmic electrodes, that have been treated separately one from another, based on a single principle that allows understanding them consistently. More specifically, the present invention is directed to overcoming the problem of uncontrollability of pinning of Fermi level of the interface of metal/semiconductor that has been impossible to control conventionally.

Therefore, an object of the present invention is to provide a method for fabricating Schottky electrode or Ohmic electrode formed at the interface between an electrode metal/semiconductor, which enables freely controlling electric properties of the electrode formed on the semiconductor.

Another object of the present invention is to provide an electrode structure comprising an electrode having a controlled Schottky barrier height of the interface between the electrode metal and the semiconductor.

According to a first aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

decreasing a surface states density of the surface of the semiconductor.

According to a second aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

controlling a Schottky barrier height of a rectifying Schottky electrode formed on the surface of the semiconductor.

Here, the control of the Schottky barrier height of the Schottky electrode may be carried out by controlling flatness of an electrode metal/semiconductor interface.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling a step density on an atomic level of an electrode metal/semiconductor interface.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling selecting a work function of the metal.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling the Schottky barrier height of the Schottky electrode under conditions without giving thermal hysteresis.

According to a third aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

fabricating a Schottky electrode from a metal having a high work function, and fabricating an Ohmic electrode from a metal having a low work function, for an n-type semiconductor, or fabricating a Schottky electrode from a metal having a low work function and an Ohmic electrode from a metal having a high work function, for a p-type semiconductor.

Here, the method may further comprise the step of heating.

According to a fourth aspect of the present invention, there is provided a method of fabricating an Ohmic electrode, comprising the step of: forming flat electrode metal/semiconductor interface on an atomic level.

According to a fifth aspect of the present invention, there is provided a method of fabricating an Ohmic electrode, comprising the step of: forming an electrode metal/semiconductor interface having a low step density on an atomic level.

According to a sixth aspect of the present invention, there is provided a method of fabricating an electrode, comprising the step of:

fabricating an Ohmic electrode as described above in a highly integrated electronic device.

Here, the semiconductor may be made of a semiconductor selected from the group consisting of Si and SiC.

The electrode metal may be selected from the group consisting of Al, Au, Mo and Ti.

According to a seventh aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor having an interface portion which is flat on an atomic level.

According to an eighth aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor having a Schottky barrier height which is impossible to realize by conventional method.

According to a ninth aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor containing no high concentration impurity.

According to a tenth aspect of the present invention, there is provided an Ohmic electrode structure having a Schottky barrier height which is substantially zero.

Here the semiconductor may be made of a semiconductor selected from the group consisting of Si and SiC.

The electrode metal may be selected from the group consisting of Al, Au, Mo and Ti.

According to an eleventh aspect of the present invention, there is provided a method of fabricating an electrode, comprising the step of

oxidizing a surface layer of silicon or silicon carbide on a surface of a semiconductor and removing the resulting oxide film

Here the oxidizing of the silicon or silicon carbide may be carried out by heating the silicon or silicon carbide in an oxidative gaseous atmosphere.

Removing the oxide film may be carried out by reacting the oxide film with a reducing liquid or gas.

The silicon or silicon carbide may be n-type silicon or n-type silicon carbide, and wherein the electrode metal is a metal having a work function lower than that of noble metals.

The silicon carbide may be p-type silicon carbide, and wherein the electrode material is a noble metal or a metal having a work function of a level substantially equal to that of noble metals.

The electrode material may be titanium (Ti).

The electrode material may be aluminum (Al).

The above and other objects, effects, features and advantages of the present invention will become more apparent from the following description of the embodiment thereof taken in conjunction with the accompanying drawings.

Fig. 1 is a graph plotting Schottky barrier height of a Schottky electrode fabricated on an n-type Si(001) substrate by a conventional method against the work function of the electrode metal;

Fig. 2 is a graph illustrating regions representing Schottky barrier heights realized by the fabrication method of the present invention.

Fig. 3 is a graph illustrating current-voltage characteristics of Ti electrodes on SiC according to examples of the present invention.

Fig. 4 is a graph illustrating current-voltage characteristics of a Ti electrode on SiC which has been subjected to a conventional treatment with 5% hydrofluoric acid;

Fig. 5 is a graph illustrating current-voltage characteristics of an Al electrode on SiC according to the present invention.

Fig. 6 is a graph illustrating current-voltage characteristics of Al electrodes on SiC according to the present invention.

Fig. 7 is a graph illustrating current-voltage characteristics of an Al electrode on Si(111) which has been subjected to a conventional treatment with 5% hydrofluoric acid;

Fig. 8A is a sketch prepared based on an optical micrograph of the surface of a Ti electrode fabricated by the fabrication method according to EXAMPLE 4 of the present invention;

Fig. 8B is a schematic cross sectional view showing the Ti electrode illustrated in Fig. 8A;

Fig. 9A is a sketch prepared based on an optical micrograph of the surface of an Ni electrode fabricated by a conventional fabrication method;

Fig. 9B is a schematic cross sectional view showing the Ti electrode illustrated in Fig. 9A;

Fig. 10 is a graph illustrating logarithmic current-voltage characteristics of Au electrodes on 6H-SiC(0001) substrates according to EXAMPLE 7 of the present invention;

Fig. 11 is a graph plotting Schottky barrier height of electrode metals fabricated on 6H-SiC(0001) substrates against the work function of the electrode metals; and

Fig. 12 is a graph illustrating new areas for Schottky barrier heights of electrode metals fabricated on 6H-SiC(0001) substrates using the techniques of the present invention.

In order to solve the problem of uncontrollability of Schottky barrier height, it is only necessary to decrease the interface states density of the interface between an electrode metal and a semiconductor on which the electrode metal layer is formed. According to the present invention, a decrease in the interface states density is realized by decreasing the surface states density of the semiconductor before deposition of a metal thereon. The decrease in the surface states density can be realized primarily by flattening the surface of a semiconductor on an atomic level.

Flattening of the surface of a semiconductor results in a decrease in an atomic step density which generates dangling bond density which is a cause of surface states and in an amount of unstable atoms adsorbed on the surface of the semiconductor. According to the present invention, it has been found for the first time that flattening of the surface of a semiconductor on an atomic level decreases the surface states density of the semiconductor and that a decrease in the surface states density is effective for decreasing the interface states density of the electrode metal/semiconductor structure.

Recently, the technology of flattening the surface of semiconductors on an atomic level has developed rapidly and a variety of methods have been proposed. The present invention uses the newest known atomic level surface flattening

technologies to demonstrate the above effect. However, the present invention should not be construed as being limited to specific atomic level surface flattening techniques. There have been known several important techniques for flattening surfaces of semiconductors on an atomic level, all of which have been proved useful in decreasing interface level density according to the present invention.

The present invention is based on a principle contrary to the conventional method in which particularly in the case of Ohmic contact, the desired Ohmic contact has been realized by intentionally decreasing ideality of interface, i.e., abruptness of structural connection.

Description will be made on how to flatten the surface of a semiconductor on an atomic level. An example of such a method is to set up conditions of oxidation appropriately so that oxidation can proceed flat on an atomic level, thus making the surface of the semiconductor after etching more flattened than the original surface.

Another method is a treatment with dilute hydrofluoric acid adjusted to have an appropriate pH. The pH of the solution can be rendered alkaline with ammonia water. Such a solution has an activity of flattening the surface of a semiconductor on an atomic level by means of a weak etching action of a lot of OH groups contained in the solution. Similarly, a semiconductor may be immersed in boiling water. This method can flatten the surface of a semiconductor on an atomic level by means of a weak etching action of deionized water.

High temperature heat treatment in hydrogen gas is also effective for flattening the surface of a semiconductor. Homoepitaxial growth can accelerate surface migration of atoms at relatively low growth rates to flatten the surface of crystal growth. As the last example, a method utilizing electromigration can also be used for flattening the surface of a semiconductor on an atomic level. Electromigration is a phenomenon in which upon application of electric current to a sample, surface atoms will migrate in a direction the same as or opposite to the direction in which electric current flows. Use of this method semiconductor surfaces can be flattened depending on the conditions. The present invention is not limited to the above-described specific methods. Instead, any method that can flatten semiconductor surfaces on an atomic level may be used similarly and will be effective for decreasing interface levels.

Hereinbelow, the idea of flattening semiconductor surfaces on an atomic level will be described in more detail. To be flat on an atomic level means existence of wide flat terraces when viewed on an atomic level. This directly indicates that an atomic step density is low in the surface concerned. Atoms at a step generally have more dangling bonds than atoms on a terrace. While the dangling bonds on a terrace will disappear after the formation of an interface with a metal due to bonding with the metal, the dangling bonds at a step will not disappear completely because of the step or difference in height as high as the thickness of one atomic layer. Therefore, after the formation of an interface, a main cause of generation of interface states is dangling bonds at steps. In other words, a decrease in a step density will result in a decrease in an interface level density. Hence, in order to decrease an interface states density, it is sufficient to flatten the surface of a semiconductor so that its step density can be decreased. Thus, even if the surface is not flattened when viewed on a scale on the order of micrometers, existence of wide terraces in more minute regions will suffice for decreasing interface states. Therefore, electrode structures with an interface having wide terraces on an atomic level, even though they have uneven or rough surfaces when viewed in a broader region, will cause a decrease in surface states density and, hence, fall within the scope of the present invention as defined below in appended claims.

If the interface states density is reduced enough by one of the above-described methods, the pinning of Fermi level will disappear. On such a pinning-free interface, what determines its potential barrier is merely a difference between respective Fermi levels, i.e., a difference between respective work functions, of the metal and the semiconductor. In this case, Schottky-Mott model expressed by equations (1) and (2) above is followed. Therefore, in the case of an n-type semiconductor, use of a metal having a high work function results in the formation of a Schottky barrier while use of a metal having a low work function gives rise to an Ohmic contact. To control the Schottky barrier height, it is only necessary to select an appropriate metal with regard to work function. For p-type semiconductors, the same idea as that for n-type semiconductors can be applied except that relationship of the magnitudes of the work functions should be reversed.

According to the present invention, the Schottky barrier height of a semiconductor can be expanded to a minimum value of 0 eV (cf. Fig. 2, region (I)) and a maximum value equivalent to the bandgap (cf. Fig. 2, region (II)).

Also, controlling the degree of pinning will in effect vary the Schottky height and, hence, controlling interface level density will enable the Schottky barrier height even when the same metal is used. That pinning can be controlled means that the Schottky barrier height can be controlled at will for each metal. As a result, the region where the Schottky barrier height can be controlled is expanded to regions (III) and (IV) in Fig. 2.

As described above, the present invention has made it possible to expand the region where the Schottky barrier height can appear from region (1) to regions (I) to (IV) in Fig. 2. Therefore, for a given metal, electrodes having the Schottky barrier heights within one of the regions (I) to (IV) also fall within the scope of the present invention. The present invention is generally applicable and operable regardless of the kind of metal and for all n-type and p-type semiconductor substrates, can be set up the regions (I) to (IV) as illustrated in Fig. 2 according to the present invention. Table 1 above indicates the Schottky barrier height regions of the present invention for representative semiconductor materials.

Another important feature of the present invention is that control of Schottky/Ohmic property can be performed without heat treatment. However, if heat treatment is carried out after the deposition of electrode metals, still a flat interface can be obtained since originally a flat surface on an atomic level is provided, an interface reaction between the metal and the semiconductor occurs uniformly in the interface therebetween. Therefore, the present invention is also effective to electrodes which are subjected to heat treatment.

While not intended to be bound thereto, the present invention can be applied suitably to fabrication of electrodes on silicon carbide (SiC). While SiC is a material with which p- and n-type semiconductors can be used with ease, they have various excellent physical properties such as large a large bandgap. The present invention will be explained further taking SiC as an example. Since in the present invention, processes are used that do not involve heat treatment, no appreciable interface chemical reaction does occur between the metal and the semiconductor. Therefore, the resulting interface receives the conditions of the surface of the semiconductor without any change, and the interface has electrical characteristics which depend on structural and chemical properties of the surface of SiC before the deposition of the electrode metal. In other words, control of the conditions of the surface of SiC makes it possible to control electric properties freely.

When no treatment is performed on the surface of SiC, a natural oxide film is formed thereon. Also, a lot of water and/or impurity atoms are adsorbed on the SiC surface. Further, in the case of as ground surfaces, there are near the surface a lot of impurity atoms contaminating or defects induced upon grinding. Such conditions depend strongly on the process by which the SiC surface is fabricated so that the resulting surface does not always have the same surface atomic conditions and surface electronic state and then unstable.

In the present invention, a method is used which depends strongly on the conditions of surface atoms as described above. Therefore, such an unstable surface layer must be removed. For this purpose, SiC is oxidized and then the resulting oxide film is removed. The oxidation and removal of the oxide film may be performed simultaneously.

As a specific example of oxidation method for oxidizing silicon carbide (SiC), there can be used a method in which SiC is heated in an oxidizing gas atmosphere. The oxidation can be carried out at a heating temperature within the range of usually 800 to 1,250°C, preferably 950 to 1,150°C.

Concerning the selection of metals for use as an electrode material, a lot of metal materials with which Ohmic electrodes have not been realized by the conventional high temperature heat treatment can be used for forming Ohmic electrodes according to surface condition controlling technique in the fabrication method for fabricating electrodes on SiC according to the present invention. Properly speaking, a theoretical approach for realizing an Ohmic contact for n-type semiconductors is to use metal materials having a low work function. However, conventionally, Ohmic contacts were obtained by coarsening or roughening the interface by means of high temperature heat treatment to provide the interface with a non-ideal (non-uniform) structure and metal materials having a high work function which are difficult to oxidize were used in order to prevent the high temperature oxidation. On the contrary, in the present invention, heat treatment does not have to be done so that the interface is abrupt enough to be ideal one and then it is possible to realize an Ohmic contact for those metal materials which do not have high work function naturally. Here, metals which do not have high work functions are those metal materials composed mainly of elements other than noble metals (Ni, Pd, Pt, Cu, Ag, and Au) having high work functions, such as Ni which has been used conventionally. More specifically, a wide variety of metals can be used, including, for example, Mg, Ca, Sr, Ba, Sc, Y, La, Ti, Zr, Hf, V, Nb, Ta, Cr, Mn, Re, Fe, Al, Ga, In, Tl and the like. Among these, those metals having not so high an oxidizing capability, e.g., Ti and Al, are preferred.

In order to realize Ohmic contacts with p-type semiconductors, theoretically, metal materials having high work functions should be used. Conventionally, however, Ohmic contacts were formed by addition of impurities in high concentrations and, hence, aluminum (Al) has been used as an electrode metal because it can serve as a p-type impurity. However, Al has a low work function and is not suited as a metal for p-type metals. In the present invention, metals having high work functions are used. More specifically, metals which can be used for p-type semiconductors for forming Ohmic contacts include noble metals such as Ni, Pd, Pt, Cu, Ag, and Al and metals having approximately the same work function as the noble metals, such as Co, Rh, Ir, Ru, Os, and Re.

In the case of n-type SiC, if heat treatment is required after the formation of electrodes, a metal which is resistant to oxidation and has a high work function can be deposited on the above-described electrode metals having low work functions to prevent oxidation of the electrode portions. Similar effects can be obtained by depositing two or more metals having low work functions on a metal forming a metal semiconductor interface. Therefore, if heating is needed or desired, the above-described effect of the present invention cannot be deteriorated. What is important in the present invention is to use a metal having a low work function for an n-type SiC and a metal having a high work function for a p-type SiC. Practically, metals are divided into low and high work function metals when they have work functions up to 4.5 eV or higher than 4.5 eV. However, 4.5 eV is not a strict threshold value. This is because when a metal is deposited on SiC at ambient (room) temperature, e.g., about 20°C, mutual diffusion of the atoms constituting the metal and the atoms constituting the SiC semiconductor may occur on the metal/semiconductor interface and effective work function alters, if the metal used is highly reactive. So, 4.5 eV is to be understood to be a practical standard for classifying

metals

More specifically the present invention comprises an oxidation process using an oxidative gas. Usually, a sample is placed in an oxidative atmosphere in an apparatus which enables heating of the sample, such as electric oven, and the sample is heated at a temperature within the range of 800 to 1,250°C. With this treatment, the surface of the sample becomes insulating due to formation of an oxide film thereon and a sufficient electric contact is not achieved. Then, the oxide film is removed with a reducing liquid or gas. It is often the case that the atoms on the surface of SiC are arranged or accumulate in a manner different from that the atoms in the bulk of the SiC. The oxidation process in an oxidative gaseous atmosphere is meant to oxidize such a denatured surface layer and make the surface layer ready to be removed by a liquid process including dissolving the surface oxide layer with a reducing liquid to remove it, or gaseous process involving reducing the surface oxide layer with a reducing gas to convert the oxide layer to a semi-conductor of non-oxidized state.

In conventional processes for fabricating electrodes, immersion or dipping of a semiconductor in a dilute hydrofluoric acid has been conducted to remove spontaneous oxide film on the surface of SiC. However, no intentional or artificial oxidation of SiC has been performed so that the unstable surface layer has not been removed completely, thus failing to provide stable Ohmic contacts.

According to the present invention, development of Schottky and Ohmic electrodes, which has heretofore been made relying on experience or empirical rules, can be made in a shorter time than before since the present invention is based on a systematized knowledge. Thus, efforts for the development of electrodes can be minimized. The method for fabricating electrodes according to the present invention does not need heat treatment, which makes a great increase in stability of the electrode structure as compared with the conventional method in which heat treatment is essential. Further, in the case of fabricating Ohmic electrodes, conventional methods use doping semiconductors with impurities in high concentrations. In the present invention, however, high concentration doping is unnecessary so that Ohmic electrodes can be fabricated simply and conveniently. In contrast to the conventional methods in which leakage current in the Schottky barrier is used, the method for fabricating electrodes according to the present invention can reduce the Schottky barrier height to zero so that high performance Ohmic electrodes having theoretically no interface resistance that has not been achieved conventionally.

According to the present invention, Schottky barrier heights, that have been almost impossible to control by conventional methods, can be controlled freely by controlling interface level density and selecting work function of metals.

In practicing the present invention, it is only necessary to make the surface of a semiconductor as flat as possible on an atomic level. There are various kinds of known techniques for flattening the surface of a semiconductor on an atomic level and all such techniques can be used in the present invention. Therefore, there is no technical difficulty in practicing the present invention and the present invention can be applied to various metals and semiconductors simply and conveniently.

Hereinafter, the present invention will be described in greater detail by examples with reference to the attached drawings. However, the present invention should not be construed as being limited thereto.

EXAMPLE 1 Confirmation of Ohmic Property (SiC-Ti Structure)

In the instant example, vacuum sublimated n-type 6H-SiC was used as a semiconductor substrate immediately after it was ground. The substrate had a carrier density of about $1 \times 10^{17} \text{ cm}^{-3}$. At this carrier density, usually, the semiconductor was not metallic and it was difficult to produce an Ohmic contact. The substrate was cleaned using methanol and trichloroethylene, and then placed in an electric oven filled with an oxygen gas atmosphere and oxidized at 300°C for 30 minutes, followed by 800°C for 10 minutes. Thus an oxide film of about 5 nm thick was formed. The substrate was dipped in 5% hydrofluoric acid to remove the oxide film.

On the thus-obtained SiC substrate was deposited titanium (Ti), which is a representative high melting metal and has a low work function. The work function of Ti was 4.4 eV, which is by 0.9 eV lower than Ni, which has conventionally been used as an Ohmic electrode and has a work function of 5.3 eV. The SiC substrate used was not heated previously. The thickness of deposited film was about 500 nm. Deposition was not carried out on the entire surface of the semiconductor but through a metal mask formed with a round hole of 0.30 mm in diameter for subsequent electrical measurements.

Fig. 3 is a graph illustrating current-voltage (I-V) characteristics of the sample taken out of the vacuum apparatus (cf. line 3a). As apparent from Fig. 3, the line 3a is a straight line. Lack of nonlinearity as shown by the straight line 3a in Fig. 3 clearly indicates that the electrode obtained is Ohmic, that is, current is proportional to voltage. The interface resistance of the resulting electrode was $6.7 \times 10^{-2} \Omega \text{ cm}^2$. The electrode made of a SiC material having a low carrier density as low as $2 \times 10^{17} \text{ cm}^{-3}$ had an Ohmic contact which had theoretically the lowest resistance.

An electrode structure was fabricated in the same manner as in EXAMPLE 1 except that no oxidative etching was conducted but only dipping in 5% hydrofluoric acid was performed (COMPARATIVE EXAMPLE 1). The comparative electrode structure showed no Ohmic property but exhibited Schottky property (Fig. 4). In Fig. 4, curves 4a and 4b

show normal and reverse direction leakage currents, respectively.

EXAMPLE 2 Confirmation of Ohmic Property (SiC-Al structure)

Next, an electrode structure was fabricated in the same manner as in EXAMPLE 1 except that instead of Ti was used aluminum (Al), which is a non-transient, low melting metal and belonging to the group (III) of the periodic table. In this case, too, was obtained an Ohmic contact similar to that fabricated in EXAMPLE 1. The work function of Al is 4.3 eV. Fig. 5 shows current-voltage characteristics of the aluminum electrode fabricated under the same conditions as the Ti electrode. Similarly to EXAMPLE 1, a line 5 representing the current-voltage characteristics of the Al electrode showed linearity and the interface resistance was about $1.4 \times 10^{-2} \Omega \text{cm}^2$. The electrode made of a SiC material having a low carrier density as low as $2 \times 10^{17} \text{ cm}^{-3}$ had an Ohmic contact which had theoretically the lowest resistance.

What is common between EXAMPLE 1 and EXAMPLE 2 is that the both metals used have work functions by about 1 eV lower than those of noble metals used as electrode metal for SiC in the conventional methods. The both metals tested here exhibited effects which attain the objects of the present invention.

EXAMPLE 3 Confirmation of Ohmic Property (Si-Al structure)

The instant example is to show that the present invention is applicable to Si substrates and also realize Ohmic contacts. As a semiconductor substrate was used an n-type Si substrate having a carrier density of $7 \times 10^{16} \text{ cm}^{-3}$. The substrate was cleaned using methanol and trichloroethylene, and then placed in an electric oven filled with an oxygen gas atmosphere and oxidized at 300°C for 30 minutes, followed by 800°C for 10 minutes. Thus an oxide film of about 50 nm thick was formed. The substrate was dipped in 5% hydrofluoric acid to remove the oxide film. The substrate thus obtained was dipped in hot water to make the surface of the semiconductor substrate flat on an atomic level. Thereafter, aluminum was deposited on the surface as an electrode metal. Fig. 6 illustrates current-voltage characteristics of the resulting electrode structure. A line 6a, which is a straight line, represents the sample with 5% hydrofluoric acid treatment. A line 6b, which is also a straight line, represents the sample with hot water treatment after 5% hydrofluoric acid treatment. A line 6c, which is also a straight line, represents the sample with 5% hydrofluoric acid treatment followed by hot water treatment. Here, by the term "hot water treatment" is meant a treatment with heated deionized water at a temperature below 100°C . From Fig. 6, it is apparent that the electrode fabricated according to the present invention has an Ohmic contact having a good linearity of current-voltage characteristics (the line 6c). Hereinafter, as illustrated in Fig. 1, no metal could provide an Ohmic contact for Si substrates without high concentration doping. In fact, a comparative sample having an Si(111) substrate which did not subjected to high concentration doping and having a carrier density of $7 \times 10^{16} \text{ cm}^{-3}$ (COMPARATIVE EXAMPLE 2) gave a Schottky barrier whose ϕ_{bn} was 0.69 eV after receiving the same 5% hydrofluoric acid treatment as in the instant example (Fig. 7). In Fig. 7, curves 7a and 7b denote current flows in normal and reverse directions, respectively. Comparing the lines 6a to 6c in Fig. 6, it is observed that according as flattening processes are added or flatness increases, current increases and contact resistance decreases. In the instant example (the line 6c in Fig. 6), the doping concentration was $7 \times 10^{16} \text{ cm}^{-3}$, at which the width of the depletion layer is sufficiently thick and no tunneling will occur theoretically. Therefore, the Ohmic property observed in the sample of the instant example is considered to be attributable to a sufficiently decreased Schottky barrier.

EXAMPLE 4 Structural Uniformity of Electrode Structure

A Ti electrode was fabricated in the same manner as in EXAMPLE 1. Fig. 8A is an illustrative view prepared based on an optical micrograph of the surface of the Ti electrode. Fig. 8B is an expanded schematic cross sectional view showing the Ti electrode shown in Fig. 8A. As COMPARATIVE EXAMPLE 3, was prepared an Ni electrode by a conventional heat treatment method. The Ni electrode fabricated by cleaning using methanol and trichloroethylene, the same n-type SiC substrate as used in EXAMPLE 1, depositing Ni thereon by vapor deposition and then heating the substrate at $1,000^\circ\text{C}$ for 60 minutes. Fig. 9A is an illustrative view prepared based on an optical micrograph of the surface of the Ni electrode. Fig. 9B is an expanded schematic cross sectional view showing the Ni electrode shown in Fig. 8A. In Figs. 8A and 9A, reference numeral 11 denotes an SiC substrate, 12 is an outline contour line of the electrode, 13 is an Ni electrode, and 14 is a Ti electrode. The both Ni and Ti electrodes were in the form of a disk of 0.3 mm in diameter. From Figs. 8A, 8B, 9A and 9B, it is apparent that the Ti electrode fabricated on SiC fabricated without heat treatment in accordance with the present invention has a high flatness in surface. The Ni electrode 13 shown in Fig. 9A has a rough surface, clearly lacking structural uniformity. In contrast, in the Ti electrode 14 of the present invention, no region is observed where surface conditions are different, and the area inside a contour line 12 of the electrode 14 is uniform in appearance and highly flat, thus presenting excellent structure for Ohmic structure. The electrode fabricated according to the method of the present invention (Fig. 8B) had a surface with an unevenness (X1) of 5 nm or

less. On the contrary, the electrode fabricated by the conventional method (Fig. 9B) had a surface with an unevenness (X2) of about 200 nm. This clearly indicates that the electrode fabricated by the method of the present invention had a surface flatness much superior to the electrode fabricated by the conventional method.

EXAMPLE 5 Dependence on Atomic Level Flattening Treatment - Epitaxial Growth

The same SiC substrate immediately after grinding as used in EXAMPLE 1 was dipped in boiling water (100°C) for 10 minutes. On the other hand, a sample was prepared by homoepitaxially growing SiC on the same SiC substrate after grinding as used in EXAMPLE 1. The sample was dipped in boiling water (100°C) for 10 minutes. Then, difference in current-voltage characteristics between the epitaxial SiC substrate and the SiC substrate immediately after grinding were examined. In the case of the epitaxial SiC substrate, an expectation will be made that flattening in surface proceeds sufficiently so that the interface level density decreases and as a result, the Schottky barrier height decreased and Ohmic property increases. In fact, the SiC substrate immediately after grinding had an interface resistance of $1.2 \times 10^{-2} \Omega \text{cm}^2$ (the line 3c in Fig. 3) while the epitaxial SiC substrate had an improved interface resistance of $6 \times 10^{-3} \Omega \text{cm}^2$ (the line 3d in Fig. 3). From this it follows that epitaxial growth is effective for flattening on an atomic level the surface of a semiconductor and for decreasing interface level density of the semiconductor.

EXAMPLE 6 Dependence on Atomic Level Flattening Treatment - pH Adjusted Dilute Hydrofluoric Acid Treatment

An oxidized/etched substrate having a current-voltage characteristics represented by the line 3a in Fig. 3 as used in EXAMPLE 1 was dipped in a pH adjusted dilute hydrofluoric acid for 10 minutes. Then, a metal was deposited on the surface of the thus obtained substrate. In Fig. 3, the line 3b represents the current-voltage characteristics of the electrode sample. In this case, the dilute hydrofluoric acid was adjusted to pH 10. Comparison of the line 3b with the line 3a shows that the interface resistance is improved to $1.5 \times 10^{-2} \Omega \text{cm}^2$. As demonstrated in the instant example, pH adjusted dilute hydrofluoric acid treatment is also effective in decreasing interface level density.

EXAMPLE 7 Fabrication of a Schottky Electrode Showing Less Leakage

Fig. 10 illustrates current-voltage characteristics of gold (Au) electrode on 6H-SiC(0001) face. Lines 10a, 10b and 10c show normal direction leakage currents and 10a', 10b' and 10c' show reverse direction leakage currents. In the case of SiC surface with usual 5% hydrofluoric acid treatment, the reverse direction leakage current was on the order of 10^{-7} A/cm^2 (line 10a'). When oxidation/etching treatment was conducted, the reverse direction leakage current was decreased to 10^{-19} A/cm^2 or less (line 10b'), thus showing a drastically improvement in leakage characteristics by 12 digits. Furthermore, with additional boiling water treatment, the reverse direction leakage current was further improved by 2 digits to 10^{-21} A/cm^2 (line 10c'). This indicates that oxidation/etching treatment and boiling water treatment which accelerate flattening of the surface of the semiconductor weaken the pinning of the Schottky barrier. To note, in the instant example, the electrode itself was subjected to no heat treatment. Therefore, the instant example clearly shows that high quality Schottky electrode can be fabricated without heat treatment of the electrode.

EXAMPLE 8 Control of Pinning and Schottky Barrier Height

Fig. 11 illustrate Schottky barrier height for various metals deposited on 6H-SiC(0001) face. The horizontal axis indicates work function of the metal. In the case of usual pretreatment with 5% hydrofluoric acid, the Schottky barrier height does not substantially depend on the work function of the metal and S factor which indicates an inclination of the line is about 0.2 (line 11a). Then, atomic level flattening of SiC was conducted by oxidation/etching treatment, $S=0.8$ was obtained, which indicates almost pinning free state (line 11b). Further, boiling water treatment gives rise to $S=1.0$, which indicates no pinning is observed (line 11c). Thus, the present invention realized pinning free state for those semiconductors which inherently show pinning. As a result, the Schottky barrier height can be freely changed merely by changing the work function of the metal as illustrated in Fig. 11 clearly. When the same metal is used, change in the process of atomic level flattening of the surface of the semiconductor results in varied Schottky barrier height. Note that for Ti electrodes, Schottky barrier heights were theoretically estimated from contact resistance values.

Fig. 12 illustrates Schottky barrier heights of Schottky electrodes fabricated on 6H-SiC(0001) substrates by the conventional method and by the methods of the examples of the present invention. For strict comparison, conventional electrodes were fabricated on clean surfaces and I-V characteristics values measured at room temperature were used. The data of the conventional electrodes exist in the region (0). Ti, Mo and Au electrodes subjected to oxidation/etching treatment and boiling water treatment according to the present invention are plotted in regions (I), (IV) and (II), respectively. The data show that the present invention made it possible to realize Schottky barrier heights beyond the lower limit (region (I)) and beyond the upper limit (region (II)) that were impossible to achieve by the conventional method.

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The Mo electrode plotted in region (IV) gives the same Schottky barrier height as that of the conventional Ti electrode having lower work function. This means that to give a certain Schottky barrier height, those metals that were considered inappropriate in view of pinning action can be used in the method of the present invention.

As described above, Schottky barrier height of semiconductors can be freely controlled according to the present invention.

Table 2 summarizes the results of examples and Comparative examples above.

Table 2

	Substrate	Electrode Metal	Treatment	Figure	Interface Resistance ($10^{-2}\Omega\text{cm}^2$)	Reverse Direction Leakage Current (A/cm ²)	Surface Unevenness (nm)
Ex. 1	SiC	Ti	A+B	Fig. 3	6.7		
				Line (a)			
C.Ex.1	SiC	Ti	B	Fig. 4			
Ex. 2	SiC	Al	A+B	Fig. 5	1.4		
Ex. 3	Si	Al	A+B	Fig. 6			
				Line (a)			
	Si	Al	B+C	Fig. 6			
				Line (b)			
	Si	Al	A+B+C	Fig. 6			
				Line (c)			
C.Ex.2	Si	Al	B	Fig. 7			
Ex. 4	SiC	Ti	A+B	Fig. 8A, Fig. 8B			52
C.Ex.3	SiC	Ni	Cleaning* Heating 1,000°C	Fig. 9A, Fig. 9B			200

Table 2 (Continued)

	Electrode		Treatment	Figure	Interface Resistance ($10^{-2}\Omega\text{cm}^2$)	Reverse Leakage Current (A/cm^2)	Surface Unevenness (nm)
	Substrate	Metal					
Ex. 5	SiC (Bulk)	Ti	A+B+C	Fig. 3	1.2		
	SiC-SiC (Epitaxial)	Ti	A+B+C	Fig. 3	0.6		
Ex. 6	SiC	Ti	A+B'	Fig. 3	1.5		
Ex. 7	6H-SiC (0001)	Au	A+B	Fig. 10		10^{-19}	
	6H-SiC (0001)	Au	A+B+C	Fig. 10		10^{-21}	
C.Ex. 4	6H-SiC (0001)	Au	B	Fig. 10		10^{-7}	
Ex. 8	6H-SiC (0001)	Ti, Mo, Ni	A+B+C	Fig. 11			

*: with methanol and trichloroethylene

The present invention has been described in detail with respect to an embodiment, and it will now be apparent

from the foregoing to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects, and it is the intention, therefore, in the appended claims to cover all such changes and modifications as fall within the true spirit of the invention.

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Claims

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1. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:
decreasing a surface states density of said surface of said semiconductor.

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2. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:
controlling a Schottky barrier height of a rectifying Schottky electrode formed on said surface of said semiconductor.

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3. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling flatness of an electrode metal/semiconductor interface.

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4. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling a step density on an atomic level of an electrode metal/semiconductor interface.

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5. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling selecting a work function of the metal.

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6. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling the Schottky barrier height of the Schottky electrode under conditions without giving thermal hysteresis.

7. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:

fabricating a Schottky electrode from a metal having a high work function, and fabricating an Ohmic electrode from a metal having a low work function, for an n-type semiconductor, or
fabricating a Schottky electrode from a metal having a low work function and an Ohmic electrode from a metal having a high work function, for a p-type semiconductor.

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8. The method as claimed in any one of claims 2 to 7, characterized by further comprising the step of heating.

9. A method of fabricating an Ohmic electrode, characterized by comprising the step of: forming flat electrode metal/semiconductor interface on an atomic level.

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10. A method of fabricating an Ohmic electrode, characterized by comprising the step of: forming an electrode metal/semiconductor interface having a low step density on an atomic level.

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11. A method of fabricating an electrode, characterized by comprising the step of:
fabricating an Ohmic electrode as claimed in any one of claim 1 to 10 in a highly integrated electronic device.

12. The method as claimed in any one of claims 1 to 11, characterized in that said semiconductor is made of a semiconductor selected from the group consisting of Si and SiC.

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13. The method as claimed in any one of claims 1 to 12, characterized in that said electrode metal is selected from the group consisting of Al, Au, Mo and Ti.

14. A Schottky electrode structure provided on a semiconductor characterized by having an interface portion which is flat on an atomic level.

15. A Schottky electrode structure provided on a semiconductor characterized by having a Schottky barrier height which is impossible to realize by conventional method.
- 5 16. An Ohmic electrode structure provided on a semiconductor characterized by containing no high concentration impurity.
17. An Ohmic electrode structure characterized by having a Schottky barrier height which is substantially zero.
- 10 18. The electrode structure as claimed in any one of claims 14 to 17, characterized in that said semiconductor is made of a semiconductor selected from the group consisting of Si and SiC.
19. The electrode structure as claimed in any one of claims 14 to 17, characterized in that said electrode metal is selected from the group consisting of Al, Au, Mo and Ti.
- 15 20. A method of fabricating an electrode, characterized by comprising the step of:
oxidizing a surface layer of silicon or silicon carbide and removing the resulting oxide film.
- 20 21. The method as claimed in claim 20, characterized in that said oxidizing of the silicon or silicon carbide is carried out by heating the silicon or silicon carbide in an oxidative gaseous atmosphere.
22. The method as claimed in claim 20, characterized in that said removing the oxide film is carried out by reacting the oxide film with a reducing liquid or gas.
- 25 23. The method as claimed in any one of claims 20 to 22, characterized in that said silicon or silicon carbide is n-type silicon or n-type silicon carbide, and wherein said electrode metal is a metal having a work function lower than that of noble metals.
- 30 24. The method as claimed in any one of claims 20 to 22, characterized in that said silicon carbide is p-type silicon carbide, and wherein said electrode material is a noble metal or a metal having a work function of a level substantially equal to that of noble metals.
25. The method as claimed in claim 23, characterized in that said electrode material is titanium (Ti).
- 35 26. The method as claimed in claim 23, characterized in that said electrode material is aluminum (Al).
27. A method of producing a Schottky diode or other semiconductor device having electrodes which includes fabricating electrodes by any method or combination of methods as claimed in any of claims 9 to 13 or 20 to 26 or which includes fabricating electrodes by patterning or fabricating in a pattern a layer of electrode metal produced by any method claimed in claims 1 to 8.
- 40 28. A semiconductor device having at least two metal electrodes formed on a semiconductor surface and wherein the flatness of the semiconductor surface is different at each interface with said two respective metal electrodes.
- 45 29. A device according to claim 28 wherein the electrodes are ohmic and Schottky electrodes respectively, and the interfaces therewith are atomically flat and other than atomically flat respectively.

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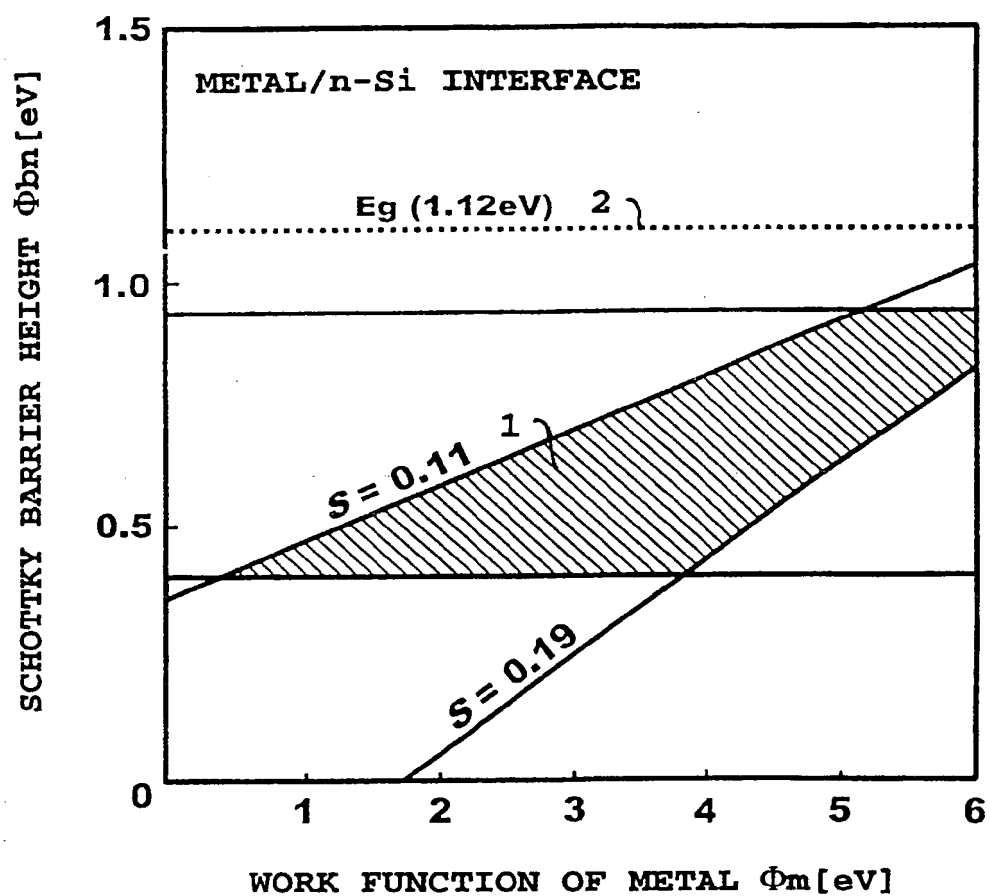


FIG. 1
(PRIOR ART)

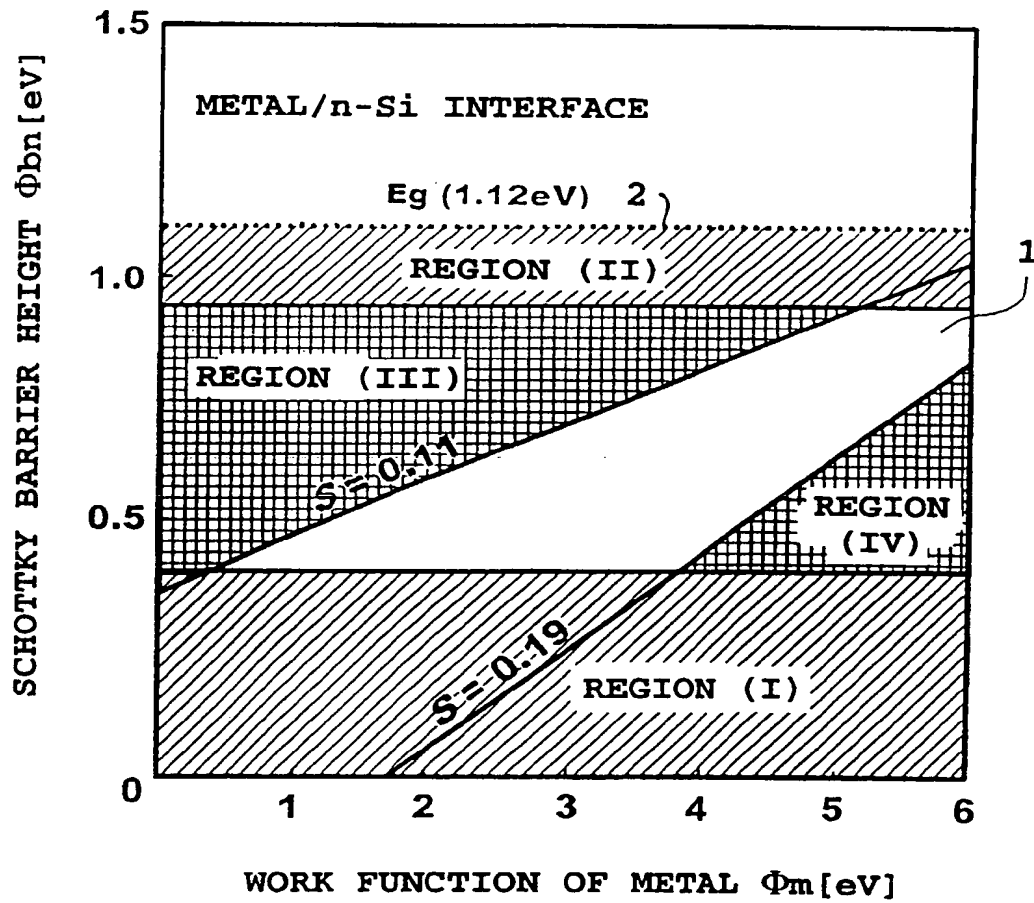
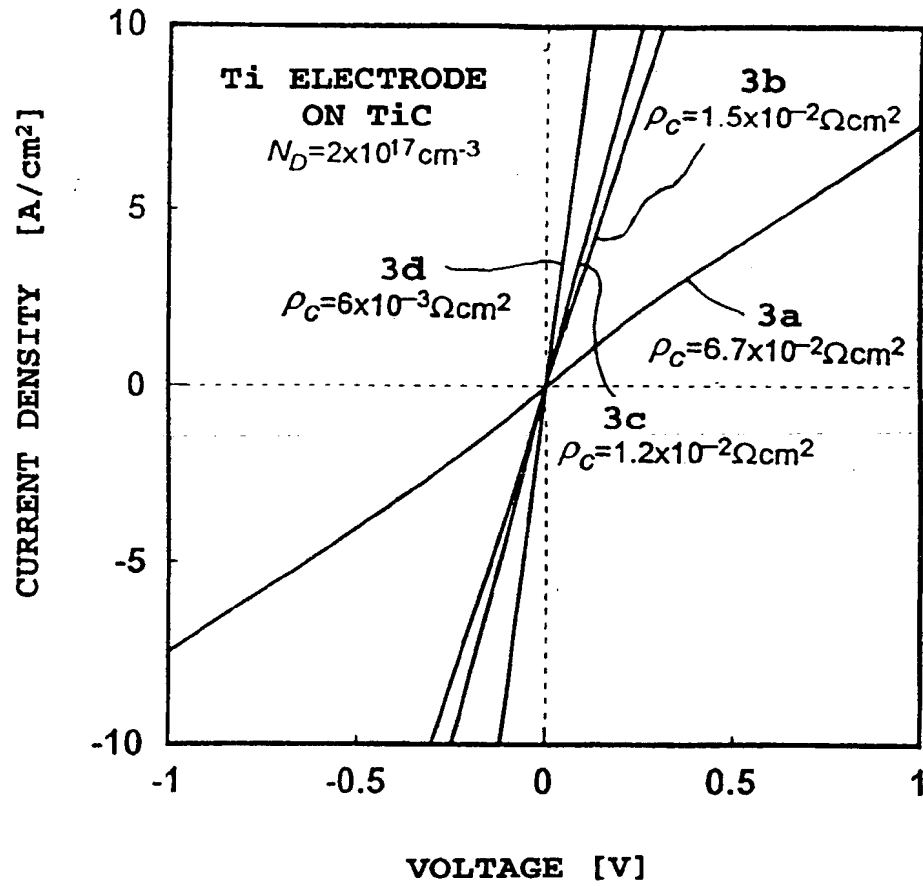


FIG. 2

**FIG. 3**

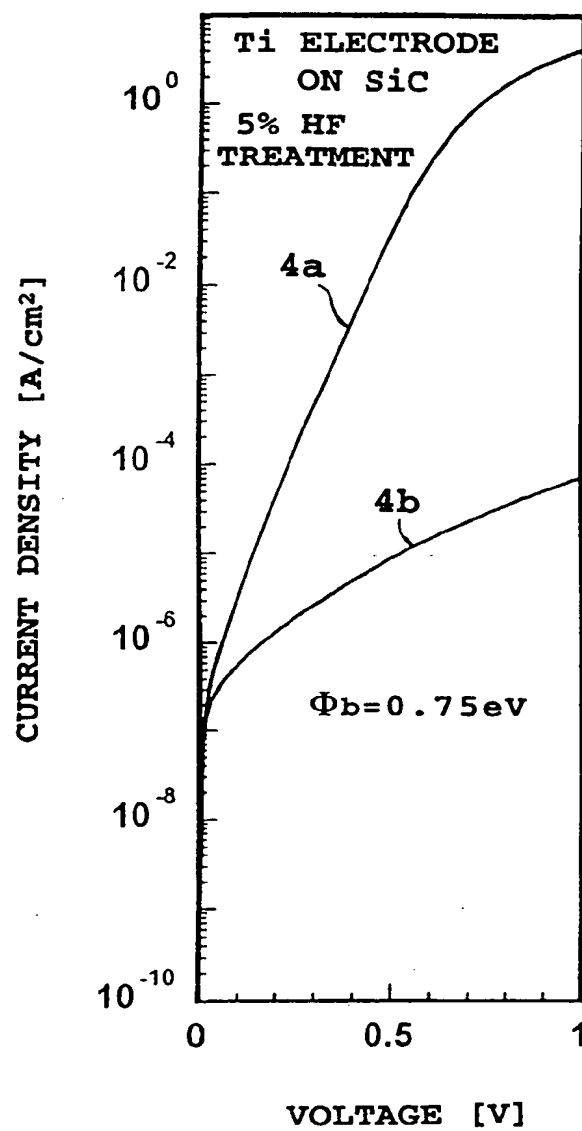


FIG. 4

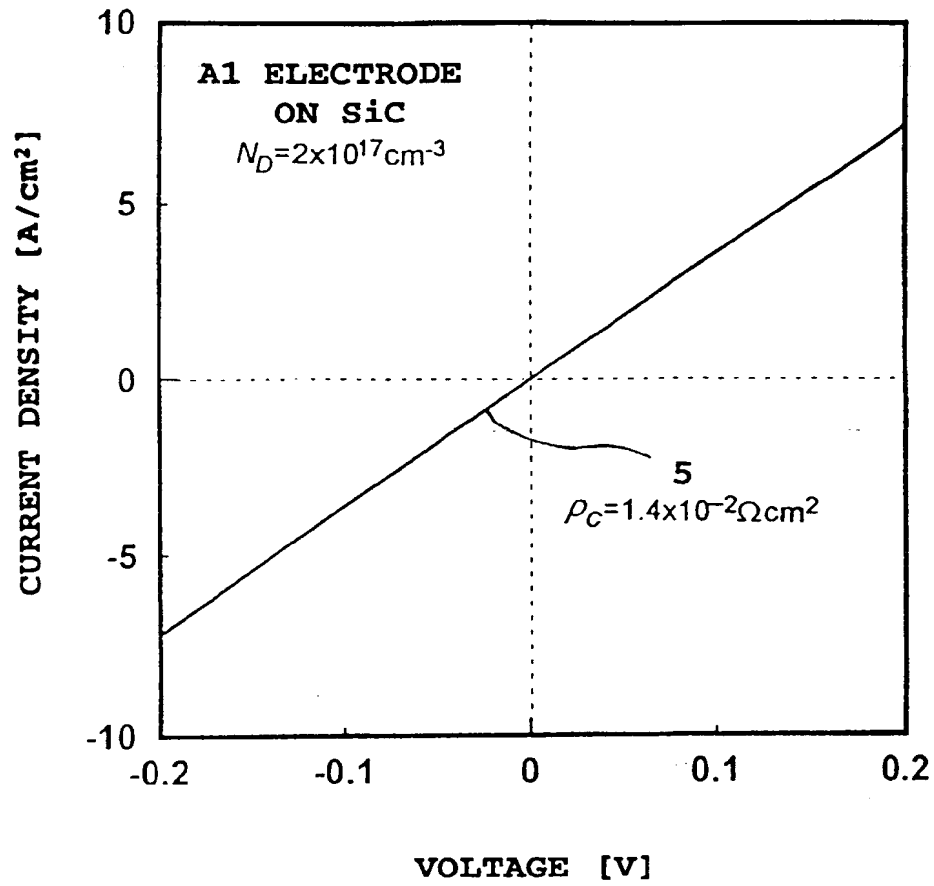


FIG. 5

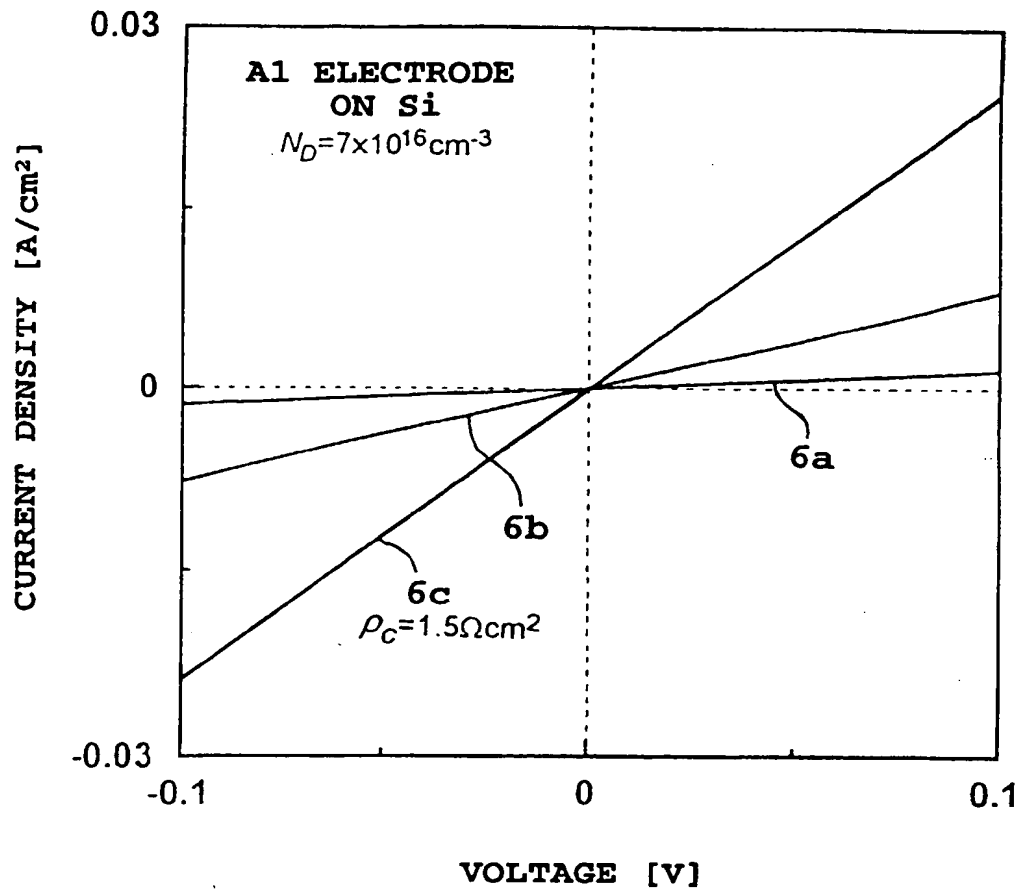


FIG. 6

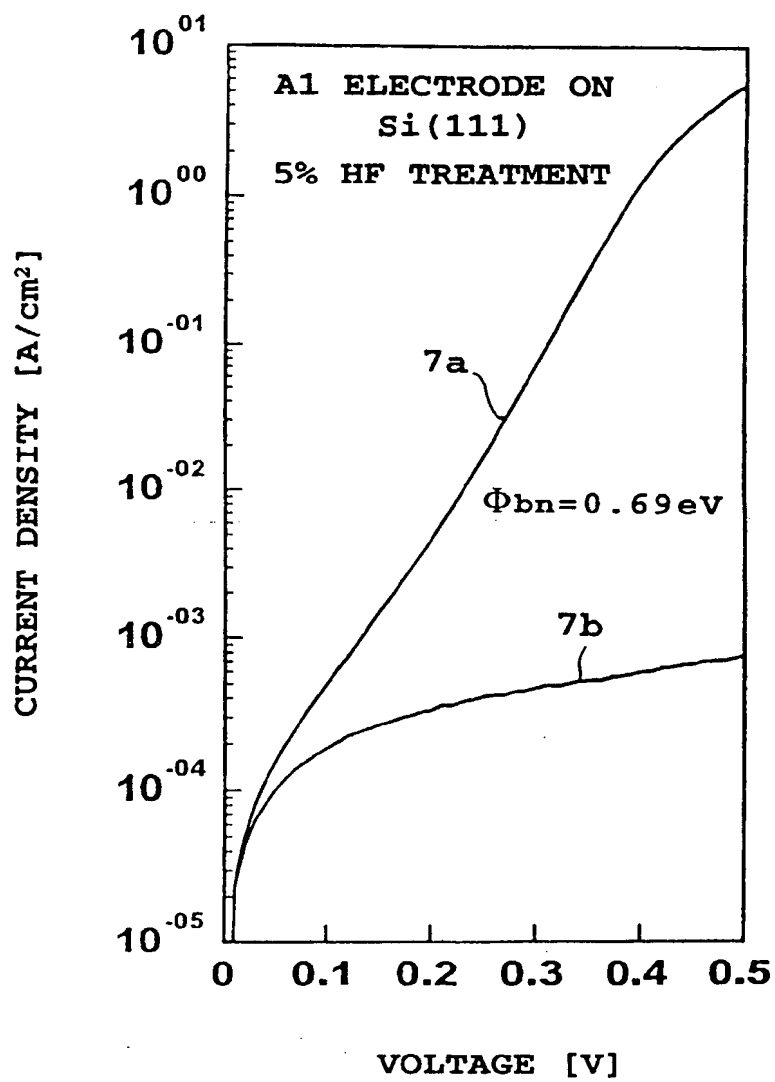


FIG. 7

FIG. 8A

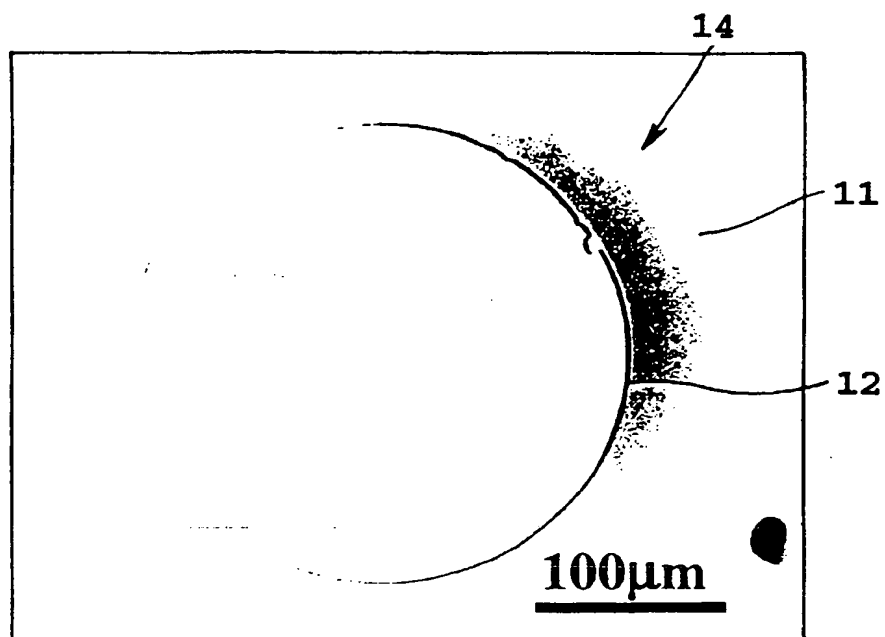


FIG. 8B

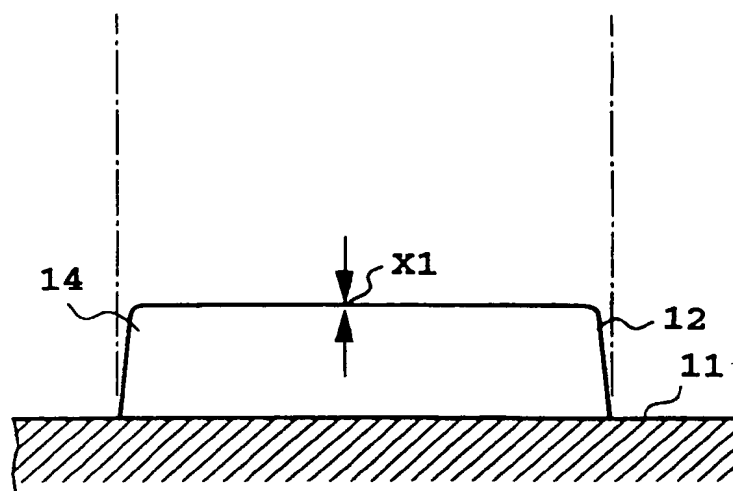


FIG. 9A

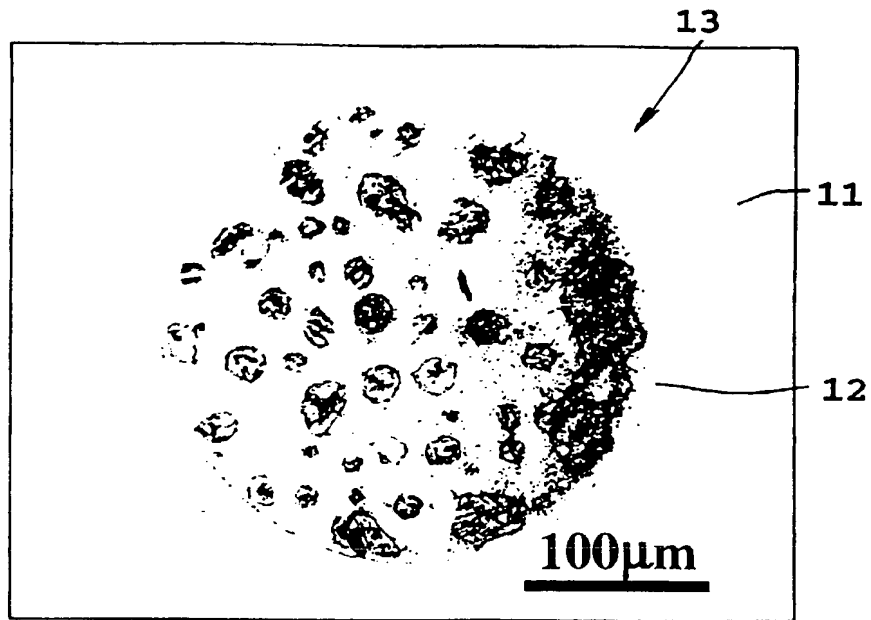
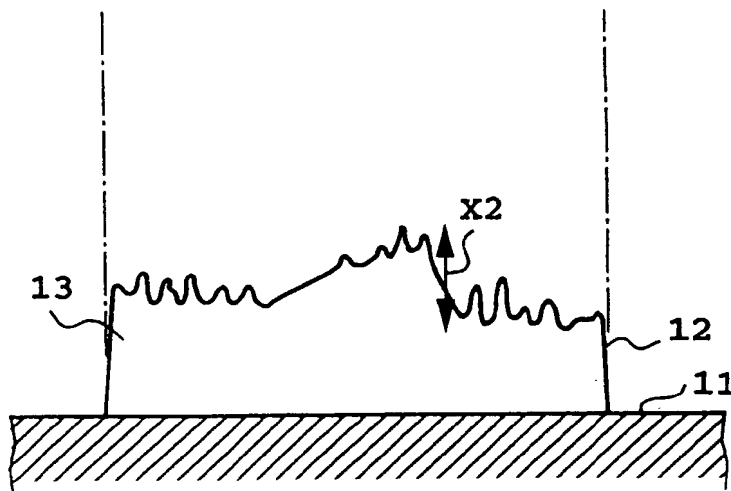


FIG. 9B



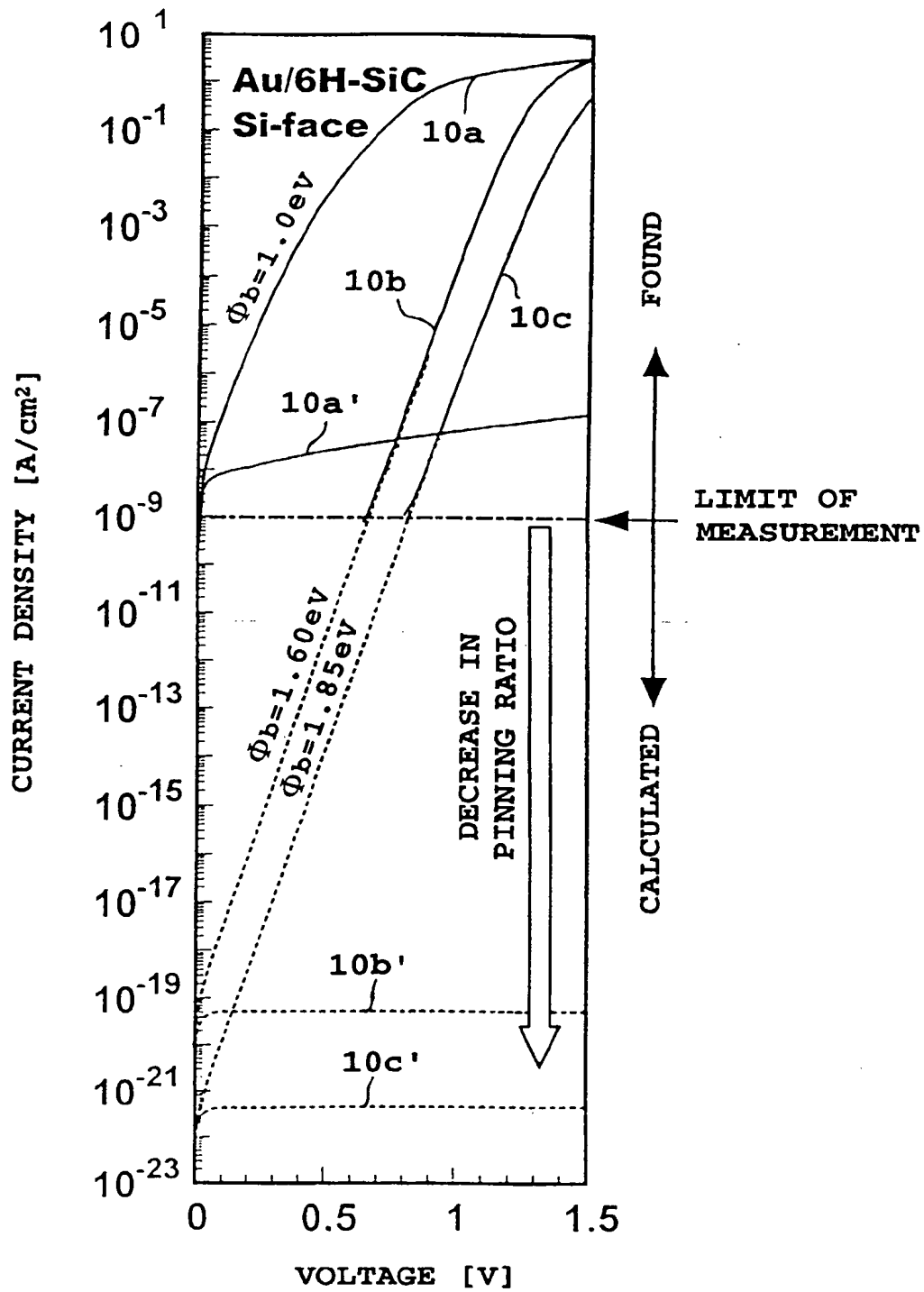


FIG. 10

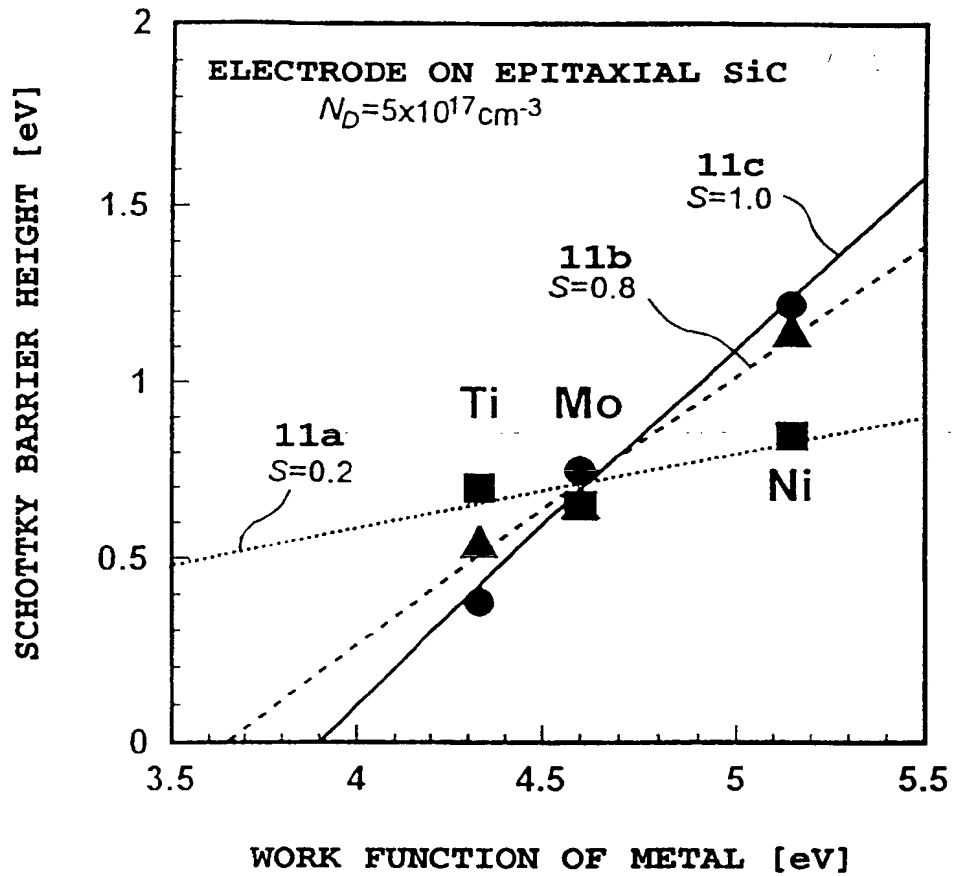


FIG. 11

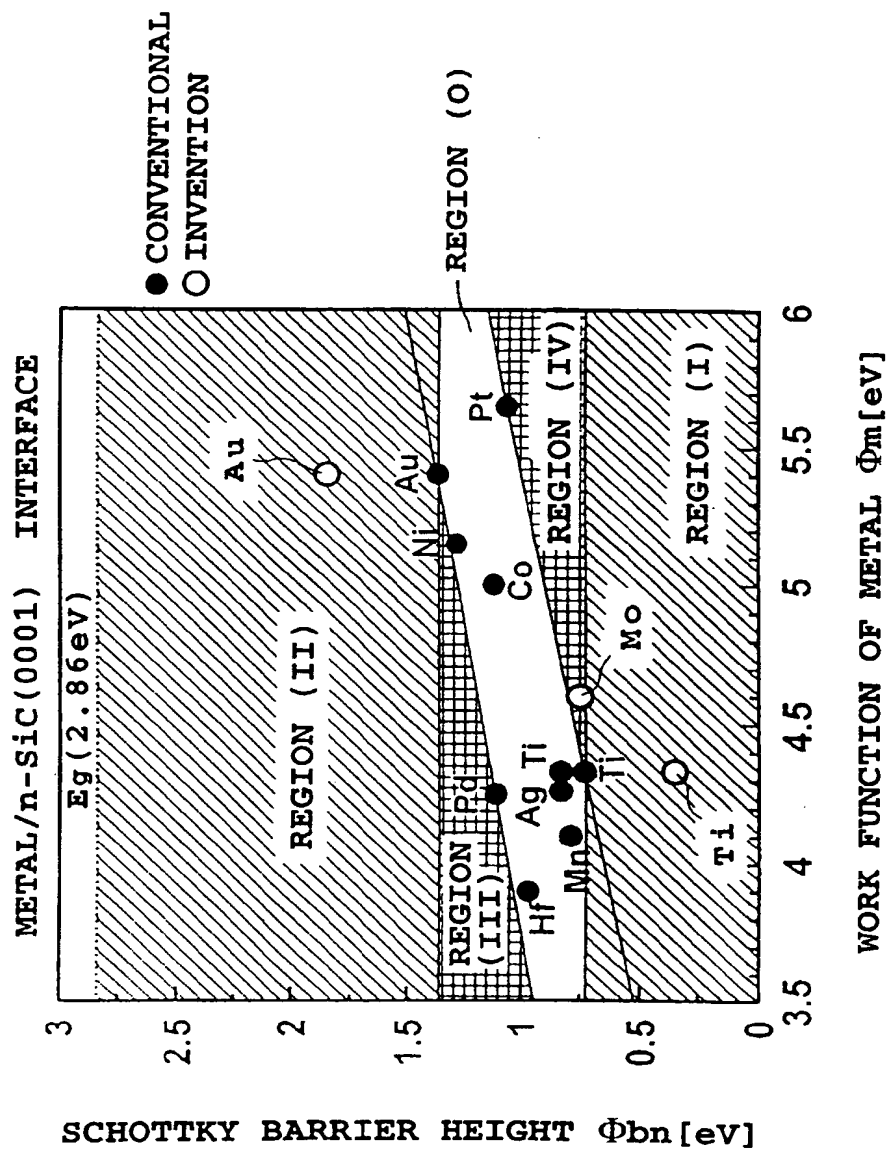
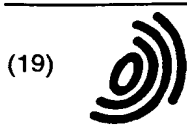


FIG.12



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(54) Structure and fabrication method for schottky and ohmic electrodes onto semiconductor devices

(57) A novel electrode structure for Schottky electrodes and Ohmic electrodes and novel methods of fabricating electrodes by freely controlling electric characteristics of electrodes on semiconductors. Interface states density of a semiconductor (11) after deposition of an electrode metal (13, 14) is decreased by flattening the surface of the semiconductor on an atomic level to freely control the Schottky barrier height. The method can realize an ideal Ohmic electrode having a Schottky barrier height of substantially zero. The Schottky barrier height is varied freely by decreasing the interface level density and selecting work function of the electrode metal. The method can provide stable Schottky and Ohmic electrodes (13, 14) without need of heat treatment. Further, the method can provide Ohmic electrodes without high concentration doping.

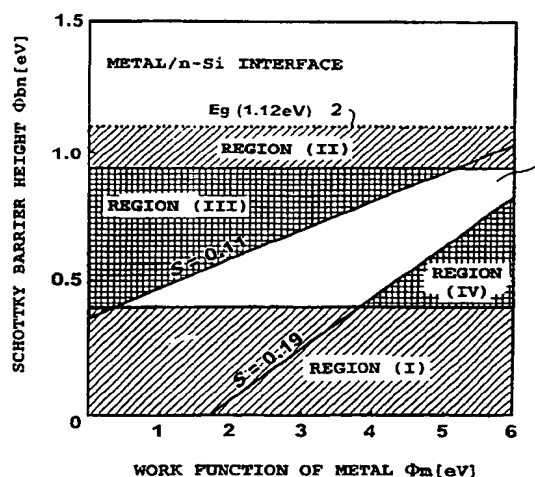


FIG. 2

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PARTIAL EUROPEAN SEARCH REPORT

Application Number

which under Rule 45 of the European Patent Convention shall be considered, for the purposes of subsequent proceedings, as the European search report

EP 96 30 6139

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	S. M. SZE: "Physics or Semiconductor Devices" 1981, JOHN WILEY & SONS, NEW YORK XP002068071 * page 245 - page 311 *	2,5,7,8,17	H01L21/285 H01L21/04
X	US 4 301 592 A (LIN HUNG CHANG) 24 November 1981 * column 2, line 63 - column 3, line 32; figures 2,3 *	1	
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X	ADEGBOYEGA G A ET AL: "SCHOTTKY CONTACT BARRIER HEIGHT ENHANCEMENT ON P-TYPE SILICON BY WET CHEMICAL ETCHING" APPLIED PHYSICS A. SOLIDS AND SURFACES, vol. A48, no. 4, 1 April 1989, pages 391-395, XP000112320 * the whole document *	20,22	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H01L
INCOMPLETE SEARCH The Search Division considers that the present application, or one or more of its claims, does/do not comply with the EPC to such an extent that a meaningful search into the state of the art cannot be carried out, or can only be carried out partially, for these claims. Claims searched completely : Claims searched incompletely : Claims not searched : Reason for the limitation of the search: see sheet C			
Place of search THE HAGUE		Date of completion of the search 15 June 1998	Examiner Königstein, C
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

EPO FORM 1503 03/82 (P4/C07)



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INCOMPLETE SEARCH
SHEET C

Application Number

EP 96 30 6139

Claim(s) searched completely:
1-5,7-14,16-29

Claim(s) searched incompletely:
6,15

Reason for the limitation of the search:

The subclaim 6 describes the fabrication of a Schottky electrode characterized in that the Schottky barrier height is controlled 'under conditions without giving thermal hysteresis'.

The claim 15 describes a Schottky electrode characterised by having a Schottky barrier height 'which is impossible to realize by conventional method'.

The wording used in these two claims is not clear (Art. 84 EPC).

In claim 6, it is not clear what (effect) gives the thermal hysteresis and how this can be achieved.

In claim 15, it is not clear what is meant with 'conventional method'.



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PARTIAL EUROPEAN SEARCH REPORT

Application Number
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A	US 4 060 820 A (PUCEL ROBERT A ET AL) 29 November 1977 * the whole document *		
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EPO FORM 1503 03.82 (P04C10)

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Office

PARTIAL EUROPEAN SEARCH REPORT

Application Number
EP 96 30 6139

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
P,X	HARA S ET AL: "Pinning-controlled metal/semiconductor interfaces" THIRD INTERNATIONAL CONFERENCE ON INTELLIGENT MATERIALS. THIRD EUROPEAN CONFERENCE ON SMART STRUCTURES AND MATERIALS, LYON, FRANCE, 3-5 JUNE 1996, vol. 2779, ISSN 0277-786X, PROCEEDINGS OF THE SPIE - THE INTERNATIONAL SOCIETY FOR OPTICAL ENGINEERING, 1996, SPIE-INT. SOC. OPT. ENG, USA, pages 802-806, XP002068070 * the whole document * -----	1,2,7	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

EPO FORM 1503 03.82 (P04C10)

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